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SUMMARY: Computer/Microcontroller Hardware and Software specialist with over 20 years of electronics experience delivering quality work in a timely manner. Extremely fast learner. Self-motivated. Product orientated. Software experience includes Microsoft Windows VB program development, Linux scripts, database creation/management, image manipulation/scaling, and system control drivers for synchronous and asynchronous I/O. HDL experience includes functional modeling, simulation, synthesis, debug, and test bench generation in Verilog and VHDL. ASIC experience includes cell/library development and characterization, and timing-driven place & route activities using Synopsys and Mentor tools. Hardware experience includes custom PAL, PLD, and FPGA development, PCB and MCM design and layout.

EXPERIENCE: Utilized high-end layout techniques to develop numerous cells and macros for the TimeLab Arbitrary Waveform Synthesizer (AWS) circuitry capable of generating 2+GHz clocks in .13u and .18u CMOS processes; judicious use of dummy structures and layout symmetry was essential to meet the pico-second jitter and skew performance goals by minimizing disruptive capacitance and on-chip variation. Drove modifications to and resolved issues with a design flow accommodating multi-VSS and multi-VDD domains where LVS and parasitic extraction of up to 6 independent domains was necessary to get sufficient isolation between the different clocks generated by the TimeLab technology; initial design flow from the CAD tool and technology vendors supported only 2 VSS domains. Wrote numerous scripts and specialized software to assist with library preparation in support of the multi-domain voltage requirements.

Completed four .18u 266+ MHz ASICs at Oak Technology utilizing the Synopsys and ICED tools. Generated the Synopsys libraries needed for each of the designs and worked with external core/IP vendors to integrate their hard and soft macros into the Oak Technology design flows/conventions. Significant library work was needed to ensure proper timing information could be extracted/generated, to optimize pin locations for the router, and to add antenna-related gate and source/drain area for each library element. Pioneered the antenna charge detection and multi-tool solution for route stitching and diode insertion to eliminate antenna violations. Developed over 20 separate tools and wrote numerous custom scripts and programs to overcome problems/inadequacies within the tool suite.

Developed several VHDL test bench generators for a CirCADian Design client who needed the flexibility of modifying the test bench in real-time during the simulation.

Wrote approximately twenty thousand lines of unique Visual Basic code to create three Microsoft Windows based CAD programs in nine months for InterChip Systems, Inc., a company specializing in MultiChip Modules and bare die. The first program scales and positions scanned bit-map (BMP) images of bare die and places these images onto a database template. The second program parses, sorts, and translates various schematic netlists to check for errors and to rearrange the data. The third program displays context-sensitive

graphics with related fields as a mechanism for capturing PCB and MultiChip Module design rules. A fourth Windows© based CAD program creates bare die component library models; the program intelligently adds wirebonds from bare die bond pads to bond pads on a PCB or BGA package. This fourth program has been incorporated into the PADS software with little modification.

Produced the hardware, packaging, and µcode for a number of products, including various Caller ID designs, for Allied Electronics. Resolved cost, quality, and offshore vs. onshore manufacturing tradeoffs.

As Product Engineer for Livingston, Inc., oversaw the development, assembly, and test of computer based welding monitors, controllers, and small single-chip measuring instruments for the resistance welding industry. Also responsible for writing I/O interface and feedback control software for these same products. Generated custom PALS and PLDS for data-logging computer based environmental control systems for Carlson Instruments. Solved serial I/O and accuracy issues.

Designed multi-layer PC Boards, MultiChip Modules, and BGAs for numerous customers using EE Designer III Schematic Capture/PC Board Layout, FastCAD mechanical CAD software, AutoCAD©, EPD©, PADS©, SPECCTRA©, and custom software.

WORK History:
2012 – 2013 Adaptronics – Altera FPGA rework and modifications for their ECU.
2009 – 2011 Engineered the rewrite of the PADS advanced tool kit into a unified tool now called AS2Pack which includes a 3D viewer, pad ring generator for ASIC designers and a basic LR extractor for the wire bonds.
2006 - 2009 Independent Contractor, Isine - Custom ASIC design & Cell Development
2004 - 2006 Principal ASIC Engineer, TimeLab Corporation - ASIC design & Cell Development
2000 - 2004 Principal ASIC Engineer, Oak Technology - ASIC design & CAD Development
1998 - Co-founder, CirCADian Design LLC - ASIC/Hardware design & CAD Development
1996 - 1998 InterChip Systems, Inc. - Software Development.
1995 - 1996 Allied Electronics - Software Development and PCB Layout.
1988 - 1995 Livingston, Inc. - Product engineer.
1986 - 1988 Carlson Instruments - Controls engineer.

DETAILS: Developed the following 5 tools for InterChip Systems and, then licensed from InterChip to PADS Software, as part of the advanced packaging tool kit for PADs Power BGA:

Component IQ: Reads in a Bitmap of a die, allows the user to graphically outline each pad on the die and annotate each pad with pad/pin information as well as general die information, and finally generates a text file which contained all the necessary information about the die and each pad including location on the die, netlist pin information, electrical characteristics, and wire bond attach points. Passive and packaged component information could also be captured by this program.

Netlist IQ: A netlist reader and translator that uses an intelligent sorting algorithm to sort a netlist by net or component. The software checks

for errors in duplicate node nets, single node nets, and invalid characters in net and component names. The various output files include a netlist report file containing statistical information about the netlist as well as netlist files sorted by net and component. The final output is a translated netlist in a specific format that could be read by several different CAD tools.
Substrate IQ: Organizes the design rules from given substrate/PCB manufacturer. The rules describe the minimum, maximum, and preferred values for a given manufacturing process as well as process capabilities and/or requirements such as stacked or staircase vias. Each manufacturing process could be represented by different files, thereby allowing the flexibility of changing or trying different processes during the initial design phase of a wire bond fan out for an MCM or BGA design. Passive and packaged component information could also be captured by this program.

Assembly IQ: Organizes the design rules from a given assembly house. The rules describe the minimum, maximum, and preferred values for a given assembly process as well as process capabilities and/or requirements such as die-to-die wirebonding. Each assembly process could be represented by different files, thereby allowing the flexibility of changing or trying different processes during the initial design phase of a wire bond fan out for an MCM or BGA design. Passive and packaged component information could also be captured by this program.

Library IQ: This is the master program that takes all the information from the above programs and parametrically generates the wire bond fan out for a given die and creates a script used by layout software to generate the layout programï¿½s library component. Since any of the files can be changed using the above tools and different parameters, several different scenarios can be played out in order to determine which die, substrate/PCB manufacturer and manufacturing process, and assembly house and assembly process should be used in developing an MCM, Hybrid, or BGA design. This capability also makes it possible to take a current design and substitute parts from different manufacturers should one part become unavailable or substitute parts as requested by the client. Of course, passive and packaged component libraries can also be generated with this program.

A sample of other VB programs written to aid in the ASIC design flow:
Pad Ring Generator: Imports an ASCII comma-separated CSV (MS Excel) file and generates all the command files needed for Synopsys Astro and ICED to create a padring. Program also generates a DXF output of the padring which can be read into AutoCAD for wirebonding trials or MS Windows programs for documentation purposes The GUI offers various options to be used during the generation process including auto padding which inserts spacer cells where needed to complete the padring. Upon completion, a report is generated giving all the statistics of the padring including the die size and number of cells by type for each side. The padring display window is color coded so it is exceptionally obvious where power, ground, spacer and standard IO cells are located and the cursor reports coordinates in microns.

Library Builder: Program takes a list of standard cells and generates all the Synopsys Milkyway and ICED script files used to manipulate the cells for multiple power domains by adding PSUB2 layers with text. CDL and Verilog netlist files are also updated to reflect the new power and ground domains.
IO Library Builder: This is a program similar to the Library Builder except it generates the scripts needed to assemble a complete IO cell for the padring library by adding a bond pad at the bottom and spacer cells to either side of the base IO cell.

RC calculator: This program was developed to calculate RC parasitics and corresponding timing values of a clock trunk but can be used for any chip traces. By entering the properties of the trace to be analyzed along with the design rules and process parameters read directly from the Astro technology files, the trace delay and loading effect of the trace could be estimated. The program is a great aid in determining the optimal width and length and routing layer for a given trace segment with specific loading and delay goals.

StarRCXT STD Cell Extraction Script Generator: Takes a library netlist, a design netlist, and generates the Synopsys StarRCXT cell script files, StarRCXT main script file, and an ICED run script. The program reduced hours of parasitic extraction and SPICE simulation times by eliminating unused cells from the design library. Easily configured to include cells not found in the processed design netlist.

AS2Pack Tool Suite: Combines most of the tools listed above into one tool suite with the addition of a 3D viewer so a wire bonded port can be view from any angle. The Wire Bond Explorer has been enhanced by allowing you to have stacked devices with wire bonds going from chip to chip as well as chip to substrate. This was a two year development process and many new features added and improved. Multiple bond locations are completely editable on a pad by pad basis. The stacked device editor allows you to place and rotate a stacked device anywhere on the base die. The tool is completely scriptable and a log file is generated as the tool is used and can be modifying for playback. The Pad Ring Explorer also puts out all the files needed to generate a pad ring in the Astro and Atoptech ASIC tools. A Power Point presentation of the Wire Bond Explorer is available along with the Fast Start document.